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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,180	08/27/2001	Hideyuki Harada	P/1071-1440	7067

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EXAMINER	
MAYES, MELVIN C	
ART UNIT	**PAPER NUMBER**
1734	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,180	HARADA ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-15 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

(1)

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

(2)

Claims 1, 6, 10-12 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin, February 1978 (entitled "Internal Capacitors and Resistors for Multilayer Ceramic Modules") in view of Mikeska et al. 5,254,191 or in view of Steinle et al. 5,876,538 and Mikeska et al. 5,254,191.

IBM Technical Disclosure Bulletin discloses a method of making a multilayer ceramic module having resistors and/or capacitors built into the module comprising: inserting a prepared capacitor element between greensheets 12, 14, the capacitor element comprising either a ceramic disk coated with sintered metallurgy 10 (terminal electrode), a ceramic disk 23 or a layer of dielectric material 25 deposited on one of the greensheets, the greensheets having metallurgy filled vias 18 (wiring conductor) in contact with the metallurgy (terminal electrodes) of the capacitor element and connecting metallurgy stripes 20; assembling the greensheets; and sintering. As shown in Figure 1, the ceramic disk of the capacitor has thickness less than the thickness of the greensheets. IBM Technical Disclosure Bulletin does not disclose providing at least one restriction layer on the assembled green sheets.

Mikeska et al. 5,254,191 teach that to reduce XY shrinkage and distortion during firing of a ceramic body such as a multilayer circuit, constraining layers of non-metallic inorganic solids

which do not sinter during the sintering of the ceramic body are provided on at least one surface of the unfired ceramic body, and after firing, the porous constraining layer(s) removed from the sintered ceramic body. Mikeska et al. teach that the use of constraining layers permits the firing of tape layers (green layers) with rigid prefired ceramic substrate while maintaining excellent XY dimensional stability in the layers (col. 2, lines 38-64, col. 4, lines 13-65, col. 13, lines 15-21).

Steinle et al. teach that a ceramic multilayer substrate is provided with integrated capacitors by providing the capacitor structure on a first green ceramic film; placing another green film thereon and pressing the films together so that the capacitor structure is pressed into the ceramic films (col. 3, line 5 – col. 4, line 10).

It would have been obvious to one of ordinary skill in the art to have modified the method of IBM Technical Disclosure Bulletin for making a multilayer ceramic module having built-in resistors and/or capacitors by providing removable constraining layers which do not sinter on the assembled greensheets, as taught by Mikeska et al, to reduce XY shrinkage and distortion during firing of an unfired multilayer ceramic body (green sheet laminate). Providing constraining layers (restriction layers) on the assembled greensheet stack including the ceramic disk(s) (prefired ceramic) would have been obvious to one of ordinary skill in the art to reduce XY shrinkage and distortion of the greensheets during the firing of the green sheets to make the multilayer module, as Mikeska et al. teach that the use of constraining layers maintains excellent XY dimensional stability of tape layers even when fired with a prefired substrate.

By arranging the capacitor element(s) and/or resistor element(s) having a fired ceramic disk between assembled greensheets, as disclosed by IBM Technical Disclosure Bulletin, an

unsintered composite laminate is provided in which a sintered plate of a first ceramic functional material is arranged between primary faces of a pair of adjacent green layers which are in substantially parallel planes, as claimed.

Providing the capacitor element between the greensheets by placing the capacitor element on one of the green sheets, placing the other greensheet thereon then pressing, as claimed in Claim 21, would have been obvious to one of ordinary skill to assemble the capacitor element between greensheets, and further as taught by Steinle et al. as the method steps used to provide a capacitor structure integrated between green sheets for providing a ceramic multilayer substrate is provided with integrated capacitors.

(3)

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin in view of Mikeska et al. 5,254,191 or in view of Steinle et al. 5,876,538 and Mikeska et al. 5,254,191 as applied to claim 1, and further in view of Branchevsky 6,252,761 and JP 10-112417.

Branchevsky teaches that since there is a practical limit to the dielectric constant that can be achieved with single layer capacitors, it is desirable to have a multilayer capacitor embedded in a ceramic block to provide increased capacitance compared to single layer capacitors (col. 2, lines 36-51).

JP 10-112417 (JP '417) teaches that a laminated capacitor having top and bottom surface electrodes can be provided as a layered product having internal electrodes connected to the surface electrodes by via holes in the dielectric layers. JP '417 teaches that such a laminated capacitor is made by laminating green sheets of thickness of about 10 micrometers coated with

conductive paste to form the surface and internal electrodes and firing (Abstract and computer translation).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the capacitor structure as a multilayer capacitor, as taught by Branchevsky, to provide increased capacitance compared to a single layer capacitor. Providing the capacitor structure having top and bottom metallurgy layers as a laminate of fired dielectric layers made from green sheets of thickness of about 10 micrometers with internal conductor between layers would have been obvious to one of ordinary skill in the art, as taught by JP '417 to provide a laminated capacitor having top and bottom surface electrodes instead of a single layer capacitor, as suggested by Branchevsky for increased capacitance. By forming the laminated capacitor from green sheets of thickness of about 10 micrometers, as taught by JP '417, the sintered capacitor obviously has a thickness less than 100 micrometers, as claimed.

(4)

Claims 9, 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied to claim 8, and further in view of JP 6-164150.

JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C (computer translation [0003], [0013]).

It would have been obvious to one of ordinary skill in the art to have further modified the method of the references as combined by providing the green sheets of composition that can be fired in the range of 900-1000°C, as JP '150 teaches that in providing a ceramic multilayer

substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C. Providing the green sheets which fire at 900-1000°C as comprised of glass and ceramic or ceramic and at least 5 weight percent glass, as claimed in Claims 14 and 15, would have been obvious to one of ordinary skill in the art, such as taught by Mikeska et al.

Response to Arguments

(5)

Applicant's arguments filed June 8, 2006 have been fully considered but they are not persuasive.

Applicant argues that IBM Technical Disclosure Bulletin only discloses inserting a preformed capacitor between vias and none of the other features of Claim 1 are described. Applicant argues that one skilled in the art would not employ a fired plated when a restriction layer is used. Applicant argues that IBM has metallic stripes in direct contact with the green layers and it is not apparent how a restriction layer would be employed.

(6)

IBM Technical Disclosure Bulletin discloses inserting a preformed capacitor between greensheets such that vias in the greensheets contact the metallurgy on the top and bottom surfaces of the ceramic disk of the capacitor. According to the present specification, "wiring conductors" is described as internal conductor films 10-12 and via hole conductors 13-15 (pg. 6, lines 3-4, lines 25-26). Thus, in IBM, a terminal electrode is in electrical contact with a wiring

conductor on a green layer since the capacitor metallurgy is in electrical contact with the metallurgy filled vias. Conductive vias are described by Applicant as "wiring conductors."

Using shrinkage constraining layers (restriction layers) as taught by Mikeska et al. 5,254,191 even when a fired capacitor is provided in a laminate of green sheets would have been obvious to one of ordinary skill in the art because Mikeska et al. teach that the use of constraining layers permits the firing of tape layers (green layers) with rigid prefired ceramic substrate while maintaining excellent XY dimensional stability in the layers, thus suggesting their use even when a previously fired ceramic is present to be bonded to the green layers during firing of the green layers. Further, although IBM discloses metallurgy stripes on the top and bottom surfaces of the greensheet laminate, shrinkage constraining layers can still be used because Mikeska et al. teach that constraining layer facilitate co-firing of top surface metallization without incurring damage thereto (col. 4, lines 46-48). The presence of top surface metallization does not prevent the use of a constraining layer to reduce XY shrinkage and distortion.

Conclusion

(7)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

(8)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
August 17, 2006